Claims

Subbl> 11 1. A circuit arrangement for controlling a starting relay of a starter for a motor vehicle internal combustion engine, having a battery (20) which is electrically connected to the starting relay (4), and having a computer (19) that is disposed in the control circuit of the starting relay (4), characterized in that between the computer (19) and the starting relay (4), a memory circuit (2) is disposed, which during a chronologically limited undervoltage of the battery (20) is embodied to maintain the existing control signal (STEN) for the starting relay (4).

1✓ 2. The circuit arrangement of claim 1, characterized in that the memory circuit (2) has a flip-flop (14, 15).

13 3. The circuit arrangement of claim 2, characterized in that the flip-flop (14, 15) is settable by means of an RC circuit (17, 18) in such a way that the starting relay (4) is set to the inactive state upon reapplication of the battery voltage (after a power failure).

14 4. The circuit arrangement of [one of the foregoing claims] claim 1, characterized in that between the computer (19) and the memory circuit (2), a locking circuit (1) is disposed.

15 5. The circuit arrangement of claim 4, characterized in that the locking circuit (1) detects the instantaneous logic state at a control input (STEN) and stores it in memory with the aid of the memory circuit (2).

16 6. The circuit arrangement of claim 4 [or 5],

characterized in that the locking circuit (1) is embodied to maintain the triggering for the starting relay (4) if the computer (19) is in a reset mode.

17 7. The circuit arrangement of [one of claims 4-6] claim 4, characterized in that the computer (19) switches the locking circuit (1) to be inactive once the undervoltage of the battery (20) is ended.

18 8. The circuit arrangement of [one of the foregoing claims] claim 1, characterized in that the computer (19) has a program with which the locking circuit (1) and/or the memory circuit (2) can be controlled.

19 9. The circuit arrangement of [one of the foregoing claims] claim 1, characterized in that the locking circuit and memory circuit (1, 2) span a voltage dip down to approximately 0 volts.

20 10. The circuit arrangement of claim 9, characterized in that voltages up to approximately 4 volts can be spanned without chronological limitation, and voltages under 4 volts can be spanned with chronological limitation.